

(19) World Intellectual Property Organization
International Bureau



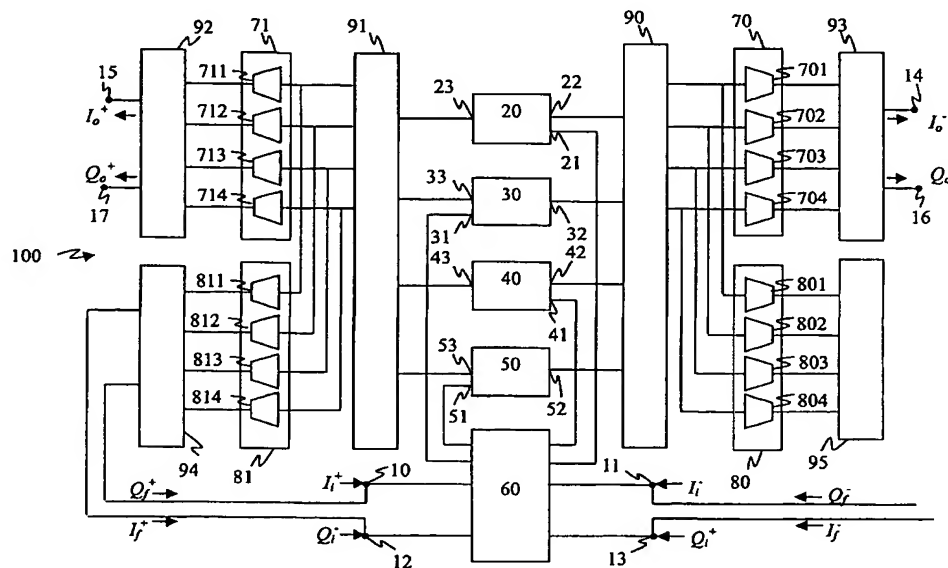
(43) International Publication Date
17 July 2003 (17.07.2003)

PCT

(10) International Publication Number
WO 03/058640 A1

- (51) International Patent Classification⁷: **G11C 27/02**, **G06G 7/18**
- (21) International Application Number: **PCT/IB02/05355**
- (22) International Filing Date:
11 December 2002 (11.12.2002)
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data:
0200289.7 8 January 2002 (08.01.2002) **GB**
- (71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]**; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): **HUGHES, John, B.** [GB/NL]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (74) Agent: **WHITE, Andrew, G.**; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:
— with international search report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: **SWITCHED-CURRENT INTEGRATOR**



(57) Abstract: A complex switched-current bilinear integrator (100) is formed as a pair of cross coupled real bilinear integrators and has inputs (10, 11, 12, 13) and outputs (14, 15, 16, 17) for differential pairs of in-phase (I) and quadrature-phase (Q) signals and an arrangement of sample-and-hold circuits (20, 30, 40, 50) and coupled scaling circuits (70, 71, 80, 81). Dynamic element matching is used to reduce the effect of mismatch between scaling circuits by interchanging scaling circuits in different signal paths. In order to prevent cross-talk of signals between different signal paths, the change of a scaling circuit coupled to a sample-and-hold circuit is constrained to occur only at the beginning of a sampling operation by that sample-and-hold circuit.